A LOW POWER, 12-BIT, 125kHz, SPLIT ARRAY-CHARGE AMPLIFIER DIGITAL -To-ANALOG CONVERTER

S. KHALDI[1], R. OUCHEN[1], R. ARNOLD[2], N. BOUGUECHAL[1], O. MANCK[2]
[1] Advanced Electronics Laboratory, Department of Electronics, Faculty of Engineering, University of Batna, Algeria
[2] Institute of Computer Engineering and Microelectronics, Technical University of Berlin, Germany
Email:madji_samia@yahoo.fr

***Abstract*-This paper presents the development and the optimisation of a high voltage, low consumption and low noise BiCMOS rail-to-rail operational amplifier.**

The developed circuit is a component of the high voltage 0.8µm BiCMOS analog library of ELMOS, especially adapted to piezoresistive Sensor Bridge used in the automotive sector [1]. This amplifier is designed to be integrated in an advanced simple and hold circuit, this amplifier, characterized by its low distortion, low noise floor. It operates as an integral part of a simple and hold circuit [2]. Simulation results have been carried out with the SPECTRE simulator using the ELMOS technology models. This rail-to-rail operational amplifier has an AC gain of 103dB, a gain bandwidth product of 764 MHz and a phase margin of 77 degree.

Keywords-***ASIC, Digital-to-Analog Converter, DAC, Split Array Charge Amplifier, High Voltage BiCMOS.***

I. NTRODUCTION

In today's world driven by fast technological developments, the present trend is towards the miniaturization of existing electronic circuits. This development will assure continuity to the products and bring improvements to conventional designs. Although the technologies evolution consists mainly in the device size decreasing, the optimal choice of a circuit design approach to achieve a specified function requires an understanding of the available liberty within the technology and the kind of devices which are easily fabricated on the integrated chip [3].

Given that the ASIC technology depends on the basic transistor type that it contains, the choice of this basic element depends on the ASIC application type, in other terms of the environment in which it will be used. Therefore, the design of the rail-to-rail operational amplifier, in the high voltage BiCMOS technology allows us to benefit the advantages of the MOS; technology such as high density and low consumption [4].

The advantage of this circuit is that due to the use of both n-channel and p-channel transistor in the two differential input pairs, the input common-mode voltage range is increased. This feature can be particularly important when low power supply volts-ages are being used. When the input common-mode voltage range is close to one of the power-supply voltages, one of the input differential pairs will turn off, but the other one will remain active. In an effort to keep the opamp gain relatively constant during this time, the bias currents of the still-active differential pair are dynamically increased. A similar situation occurs if the input common mode voltage is near the negative power-supply rail. With careful design, it has been reported that the transconductance of the input stage can be held constant to within 15 percent of its nominal value with an input common-mode voltage range as large as the difference between the power-supply voltages [6].

The idea behind the rail-to-rail structure is to use us a buffer in simple and hold circuit. This configuration has more sophisticated techniques of minimizing many properties of the circuit, including gain, speed, and noise.

In our design, the choice of this type of implementation has proved to be appropriate for our needs. The circuit structure as well as simulations evaluating its behavior are described in the remaining parts of the paper.

II. RAIL-TO-RAIL OPERATIONAL AMPLIFIER INTERNAL ARCHITECTURE

The BiCMOS amplifier shown in figure 1 has a Rail-to-rail topology, the first input stage is NMOS transistors (NM1, NM2) and the second input stage is PMOS transistors (PM1, PM2).

The bias circuit is realized using MOS transistors. It consists of a PMOS cascode current source, an NMOS cascode sink source. They are connected to provide low base currents of the input transistors. A Bias-Current cancellation technique has been applied to further reduce the operational amplifier input current [7]. The input stage consists of active loaded drain-coupled pair which is biased by a current sources of -10µA.

The outputs of the differential pairs were kept separate and not converted immediately to a single ended output. This conversion will be done later in the output stage of the amplifier.

A simple approach to extending the input common-mode range is to incorporate both NMOS and PMOS differential pairs such that when ones is "dead", the other is "alive". The idea is to combine two folded-cascode opamps with NMOS

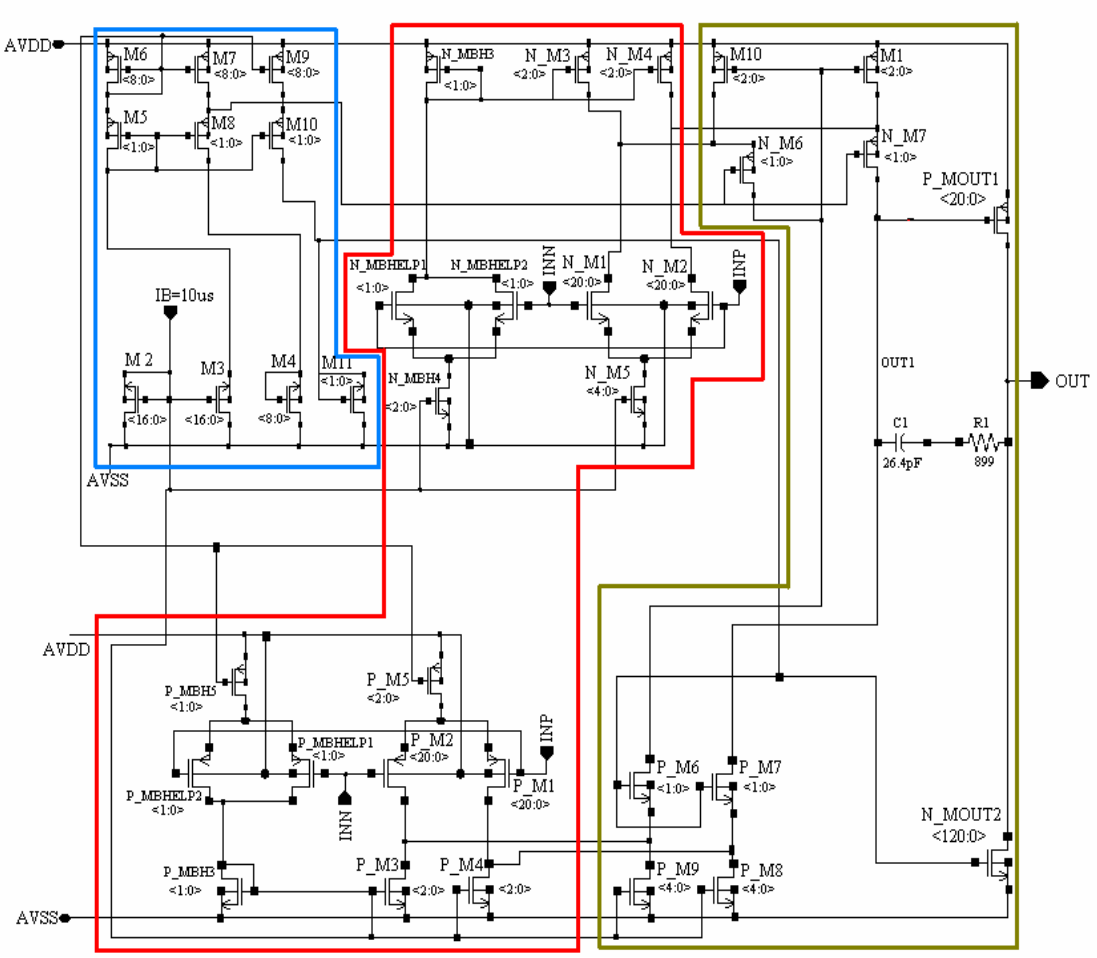

Fig. 1.Op-amp circuit diagram

and PMOS input differential pairs [5]. Here, as the input common-mode level approaches the AVSS potential, the NMOS pairs (N_M1, N_M2) transconductance drops, eventually falling to zero. Nonetheless, the PMOS pair (P_M1, P_M2) remains active, allowing normal operation. Conversely, if the input level approaches AVDD, P_M1 and P_M2 begin to turn off but N_M1 and N_M2 function properly.

In the operational amplifier output stage, the schematic shows that the Folded-Cascode topology is applied to both sides of the differential pairs. For first differential pair, The N_M1 and N_M6 transistors form a cascode structure and N_M2 and N_M7 form the other. For the second differential pair, the P_M1 and P_M7 transistors form a cascode structure and P_M2 and P_M6 form the other. The out put stage converts the differential current to a single-ended output voltage.

The operational amplifier output stage should be able to deliver substantial amount of power into a low impedance load. Therfore, it should have the following desirable properties:

1. large output current swing capability
2. large output voltage swing
3. low output impedance
4. low standby power [3], [1].

The four basic requirements for the operational output stage can be met by using a class B output stage configuration. One such possible circuit topology is the PMOS-NMOS amplifier stage shown in figure 1.

Two other differential input pairs (N_MBHELP1, N_MBHELP2) and (P_MBHELP1, P_MBHELP2) used to help the bias circuit, and a lot of current mirrors are inserted in, either as current sources or as active loads, they reflect currents between stages and improve circuit performance.

III. SIMULATION RESULTS

The SPECTRE simulations were performed for the proposed low noise rail-to-rail operational amplifier. They are based on the high voltage ELMOS BiCMOS 0.8µm technology [1].

In order to better understand and predict the circuit behavior, different analyses have been carried out.

All substrate PMOS transistors have been connected to AVDD; and all substrate NMOS transistors have been connected to AVSS.

The rail-to-rail operational amplifier offset error and gain error are shown in figure 2. The simulation of settling time is shown in Figure 3. The transient response of our circuit is shown in Figure 4.

To further characterize the amplifier, Bode plots have been done to verify its unity gain and phase margin. The simulation result in figure 4 indicates that unity-gain frequency is around 764 kHz, which meets our requirements, and the phase margin is 77 degrees. The AC gain is 103dB.

Table 1 summarizes the main simulated features of the developed Folded-Cascode operational amplifier. All the results show a good performance of our design.

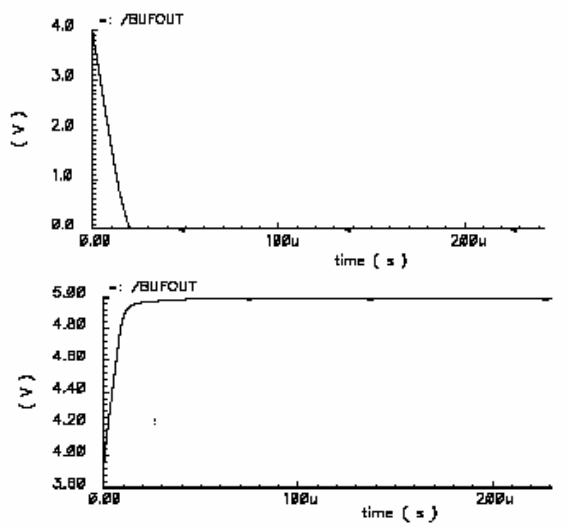

Fig. 2. The simulation result of offset error and gain error of the amplifier

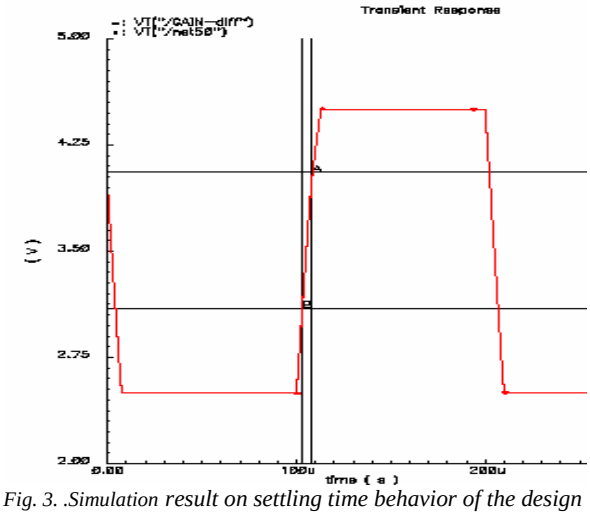

Fig. 3. .Simulation result on settling time behavior of the design

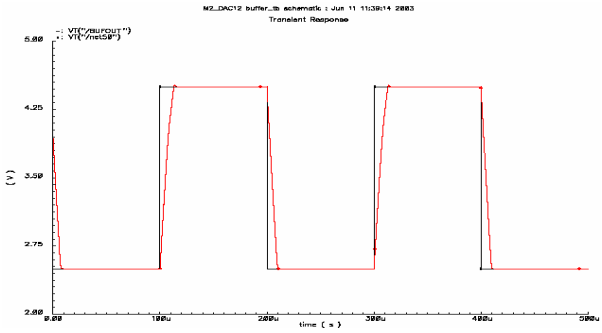

Fig. 4. Op-amp transient response

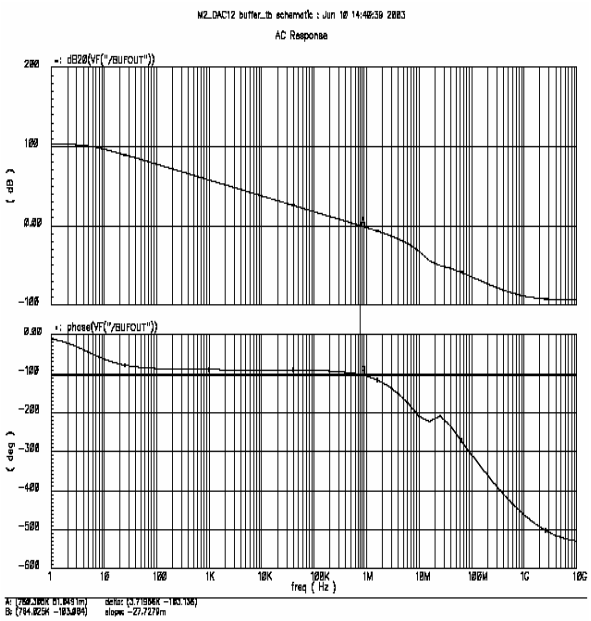

Fig. 5. Magnitude and phase Bode plot

TABLE 1. Simulated circuit specifications

Parameter design	Values
Analog power supply	+5 Volts
Offset voltage	600 µV
Erreur de gain	14 mV
Bias current (I_{BIAS})	- 10 µA
AC Gain	103dB
Unity gain frequency	764 kHz
Cut-off Frequency	5 Hz
Phase margin	77°
Settling time	2 µs

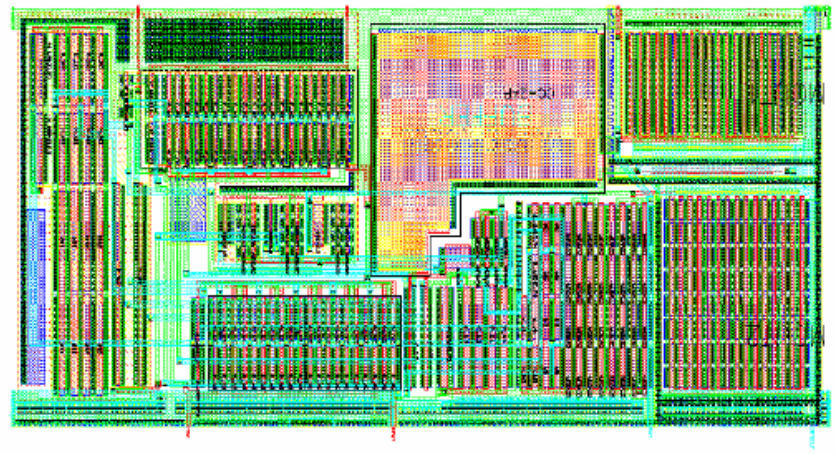

Fig.6. Op-amp layout

The design and implementation of the rail-to-rail operational amplifier is done in processes ELMOS 0.8 µm BICMOS (1 poly, 3 metals) technology [8].

When one designs analog circuits, several important layout issues should be considered to realize highquality circuits. These issues can be broadly divided into two categories matching and noise issues [4].

IV. LAYOUT DESIGN

Matching tolerances and noisy signals are minimized by appropriate layout techniques.

The layout of the rail-to-rail operational amplifier is shown in figure 6. We have built MOS transistors which represent the input stage discussed above, at the left side.

At the right, there are large MOS transistors which represent the output stage. We can also see in the top middle an attenuation capacitor.

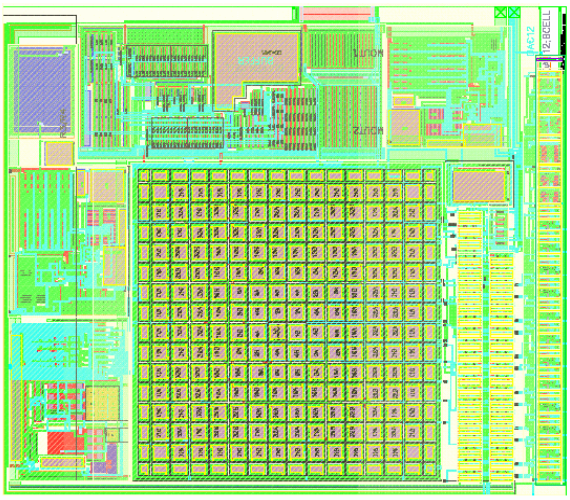

Figure 8 : Layout of the DAC

The layout of the final DAC is shown in Figure 7, and illustrates the relative size of the rail-to-rail operational amplifier which is (296.036*556.96) µm2 in relation to other components in the DAC which is (757.05*836.52) µm2.

Figure 8 shows the microphotograph of a prototype of the fabricated ASIC and illustrates the relative size of the DAC in relation to other components in the ASIC which is (3130*3270)µm2.

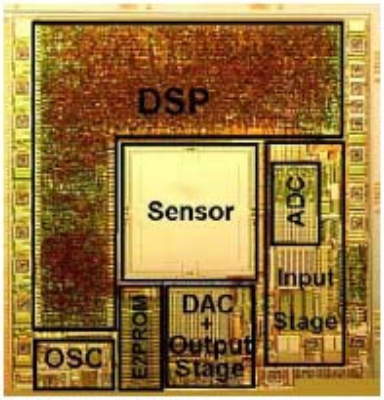

Figure 9: Microphotograph of the ASIC showing components relative sizes

V. CONCLUSION

This paper presents the development of a low noise rail-to-rail operational amplifier in the high voltage ELMOS BiCMOS 0.8µm technology. The main features of the ELMOS Bipolar/CMOS process are the high voltage capability and the combination of digital and analog functions. The integration of both NMOS and PMOS transistors within the same technology presents opportunities for significant improvement in performance over CMOS circuits design.

Simulation results using the SPECTRE simulator of CADENCE, show that the developed rail-to-rail operational amplifier satisfies chip requirements. Therefore, the integration of this library module has been achieved with success. Indeed, the technology user will have the possibility to use this component as a high performance, high voltage library element and he will be able to benefit from better performance, a reduced power consumption and a fast response.

REFERENCES

[1] *"M777.01D 2nd Order Piezoresistive Signal Processor"* Customer Detail Specification, ELMOS Semiconductor AG, 2003..

[2] Alan B. Grebene, "Analog Integrated Circuit Design", Microelectronics series. Van Nostrand Reinhold company. pp. 382-388.

[3] David A. Johns and Ken Martin, ″Analog Integrated Circuit Design″, John Wiley & Sons Inc, first edition, 1997.

[4] Behzad Razavi, ″Design of Analog CMOS Integrated Circuits″, McGraw-Hill, 2000.

[5] Robert G. Meyer, ″Analysis and Design of Analog Integrated Circuits″, 4th ed. John Wiley&Sons, Inc.

[6] D. Doyle and W.Lane, "Circuit modelling of bipolar transistors for BiCMOS", IEEEJ. Solid-state Circuits, vol. 24, pp 189-193, February 1989.

[7] Michael McCorquodale, ″CMOS Operational Amplifier Design″, EECS413 Monolithic Amplifier Circuits, University of Michigan, 1998.

[8] ELMOS Design Rule Manual of General Design Rules.